**Chip Requirements (June 11th Meeting)**

**Members in Attendance:** Dr. Pearlstein, Julie Swift and Zachary Nelson

* **Overall Goal**
  + **Produce an Audio Processing Integrated Circuit**
* I2S Interface
  + Audio Input: 2 channel stereo channel I2S (master interface)
  + Support audio input sample rates of 8kilosample/sec – 48kilosamples/sec
  + Output is the same sample rate as the input and I2S
  + Digital audio bit clock and the word select (ws) line will be controlled from master
  + Input and Output will be 2 channel 16 bits
* I2C Interface
  + Support single master configuration
  + 7-bit addressing and we will consume entire I2C address space
* Uses an external clock input
  + Clock frequency will be a minimum of 1200 times the audio sampling rate
  + Maximum clock rate will be 100 MHz
* Has an external reset pin
  + Power on reset
* Register Block
  + 512 bit frequency coefficients
  + 10k register bits
  + Register fields will include
    - Source select bit
      * Allows user to select between I2S and BIST (built in self test)
    - Filter Bypass Bit
      * 0 doesn’t bypass, 1 bypass
    - 512 16-bit signed coefficients stored as 2’s compliment
      * The effective radix point of the coefficients (4 bit number for data point, 4 bit number for coefficient)
    - Read only status register bits
      * Overflow/saturation detector – audio clipping
      * Input FIFO overrun
      * Output FIFO underrun
    - Control Bit Fields
      * 1 sticky bit to clear overrun
      * 1 sticky bit to clear underrun (stay until you clear them)
      * Clear Overflow Flag
      * Filter Order to Support
        + 9 bit number to represent 1 to 512
  + Presents an array of registers for hosts control and status monitoring (through I2C read and write operations).
* Provide built in self test function
  + Test gadgets for I2S
    - Test by converting I2S to audio coeffs
    - Audio coeffs to I2S
* Chips made by service call MOSIS
  + IBM7RF process, geometry, drawn gate length, 180nm gates, mixed signals,
  + Chip Area: no more than 3 by 3 squared mm
* Filter Audio
  + Implement an FIR filter on the input data based on the coefficients stored in the programmable registers
    - Programmable from 1-512 taps
    - Filter Order Control (9-bit number)
      * Support filter from 1-512 taps
    - Maintain intermediate precision of 4
* Produce a microcontroller platform to configure the audio input and output modules
  + UDA 1380
  + Produce a test fixture to show that the chip works
    - Sample analog audio and covert it to I2S
    - Receive I2S and convert it to analog audio
    - Allow user to create filter coeffs and upload them to the chip that was designed
    - Has to have software to configure the analog audio subsystem
    - Parametrize low pass filters, high pass, band pass, and comb filters
      * Use a button on a PSOC?
      * Could use slider on PSOC to change the frequency and upload the new coeffs to the chip
    - Create a board that we can plug the chip into to do testing
      * Bread board?
    - Will not have to design a printed circuit board for this chip